U.S. UTILITY Patent Application
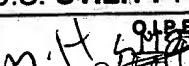
	O.I.P.E.	PATENT DATE
	M·H 5·18	
SCANNED	Q.A. 4R	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/749660		.711	141	2186	T. Thai

APPLICANTS

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TITLE

Method and apparatus for reducing memory latency in a cache coherent multi-node architecture

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL			CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

INTERNATIONAL CLASSIFICATION

☐ Continued on Issue Slip Inside File Jacket

☐ **TERMINAL DISCLAIMER**	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.

☐ The term of this patent subsequent to _____ (date) has been disclaimed.

(Assistant Examiner)   (Date)

NOTICE OF ALLOWANCE MAILED

☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____

(Primary Examiner)   (Date)

ISSUE FEE

Amount Due	Date Paid

☐ The terminal ____ months of this patent have been disclaimed.

(Legal Instruments Examiner)   (Date)

ISSUE BATCH NUMBER

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